SALAR Technologies LLC

Public Patent Portfolio Overview

This public-facing overview summarizes filed and public-safe patent areas. It avoids enabling details for active pre-filing concepts.

Patent	Status	Application / Notes
1. Board Design Reliability Analysis Checklist Guidelines	Filed; Patent Pending	U.S. Patent Application No. 18/311,244
2. Profile-Based Ethernet Connectivity for Multi-Lane SoC Devices	Filed; Patent Pending	U.S. Patent Application No. 19/433,978
3. Graph-Based Multi-Tier Semiconductor Supply-Chain Risk Scoring and Closed-Loop Mitigation	Filed; Patent Pending	U.S. Patent Application No. 19/535,459
4. Closed-Loop Manufacturing Stability Systems and Methods for Multi-Domain Control Production	Filed; Patent Pending	U.S. Patent Application No. 19/534,285
5. AI-Certified Lithography Control	In progress; public-safe summary only	Pre-filing invention | active invention in progress

Public disclosure discipline

The current public packet follows a simple rule set: the four filed lanes can be described directly; AI-Certified Lithography Control remains high-level until filing is complete; 6G is intentionally excluded from the current public packet.

Strategic center of gravity

Among the current public-safe areas, semiconductor supply-chain risk scoring functions as the center-of-gravity analytic layer, with reliability governance, interconnect profile control, manufacturing stability, and future lithography assurance feeding into a broader resilience architecture.

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